Week 5

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In this assignment, we added memory elements to the previous assignment. We added 2 memories, Program and Data Memories corresponding to ROM and RAM. These distributed memories are provided by Vivado. I made a test bench and simulated the system after joining the memories with the CPU created in Assignment 4.

For the simulation: I set reset to leading edge 1 trailing edge 0 with period 1000ns and cancel after 1000ns and for Clk, leading 1 trailing 0 with period 1000ns. For debugging I used Play for 1 Time Period.